

On page 47, line 5, delete "from left to right" and substitute -- from right to left--.

On page 47, line 8, delete "right" and substitute --left--.

On page 47, line 9, delete the first "left" and substitute --right--.

On page 49, line 22, delete "primay" and substitute --primary--.

On page 54, line 13, delete "70" and substitute --69--.

On page 56, line 2, delete "Figure11" and substitute --Figure 11--.

On page 60, line 10, after "147" insert --A, B--.

IN THE CLAIMS:

Kindly cancel claims 1-150, without prejudice.

Kindly add the following claims:

1. ~~151~~. A method of controlling a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of controlling the memory device comprises:

issuing a write request to the memory device, wherein in response to the write request, the memory device samples first and second portions of data;

providing a first portion of data to the memory device synchronously with respect to a rising edge transition of an external clock signal; and

providing a second portion of data to the memory device synchronously with respect to a falling edge transition of the external clock signal.

1 ² ~~152. The method of claim ¹ ~~151~~ wherein the write request, the~~
2 first portion of data and the second portion of data are included
3 in a packet.

1 ³ ~~153. The method of claim ¹ ~~151~~ wherein the write request, the~~
2 first portion of data and the second portion of data are included
3 in the same packet.

1 ⁴ ~~154. The method of claim ¹ ~~151~~ further including:~~
2 providing block size information to the memory device, wherein
3 the block size information defines a first amount of data to be
4 input by the memory device in response to a write request wherein:
5 a first portion of the first amount of data is
6 sampled by the memory device in response to a rising edge
7 transition of the external clock signal; and
8 a second portion of the first amount of data is
9 sampled by the memory device in response to a falling
10 edge transition of the external clock signal.

1 ⁵ ~~155. The method of claim ¹ ~~151~~ further including:~~
2 providing block size information to the memory device, wherein
3 the block size information defines a first amount of data to be
4 output by the memory device in response to a read request;
5 issuing a read request to the memory device; and
6 receiving the first amount of data from the memory device.

1 ⁶
~~156~~. The method of claim ⁵~~155~~ further including providing
2 access time information to the memory device, wherein the access
3 time information is representative of a number of clock cycles of
4 the external clock signal to delay before the memory device outputs
5 the first amount of data.

1 ⁷
~~157~~. The method of claim ¹~~151~~ further including:
2 providing the external clock signal to the memory device
3 wherein:

4 in response to a rising edge transition of the
5 external clock signal the memory device samples the first
6 portion of the data; and

7 in response to a falling edge transition of the
8 external clock signal the memory device samples the
9 second portion of the data.

1 ⁸
~~158~~. A method of controlling a memory device, wherein the
2 memory device includes a plurality of memory cells, the method of
3 controlling the memory device comprises:

4 issuing a write request to the memory device, wherein in
5 response to the write request, the memory device samples first and
6 second portions of data;

7 providing a first portion of data to the memory device
8 synchronously with respect to a first external clock signal; and

9 providing a second portion of data to the memory device
10 synchronously with respect to a second external clock signal.

1 ⁹
2 ~~159.~~ The method of claim ~~158~~ wherein the write request, the
3 first portion of data and the second portion of data are included
in a packet.

1 ¹⁰
2 ~~160.~~ The method of claim ~~158~~ wherein the write request, the
3 first portion of data and the second portion of data are included
in the same packet.

1 ¹¹
2 ~~161.~~ The method of claim ~~158~~ further including:
3 providing block size information to the memory device, wherein
4 the block size information defines a first amount of data to be
5 input by the memory device in response to a write request; and
6 wherein a first portion of the first amount of data is sampled
7 synchronously with respect to the first external clock signal, and
8 a second portion of the first amount of data is sampled
synchronously with respect to the second external clock signal.

1 ¹²
2 ~~162.~~ The method of claim ~~158~~ further including:
3 providing block size information to the memory device, wherein
4 the block size information defines a first amount of data to be
5 output by the memory device in response to a read request; and
6 receiving the first amount of data from the memory device.

1 ¹³
2 ~~163.~~ The method of claim ~~162~~ further including:
3 providing access time information to the memory device,
wherein the access time information is representative of a number

4 of clock cycles of the first external clock signal to delay before
5 the memory device outputs data.

1 ¹⁴~~164~~. The method of claim ⁸~~158~~ further including:

2 providing the first and second external clock signals to the
3 memory device, wherein:

4 the first portion of data is sampled by the memory
5 device synchronously with respect to the first external
6 clock signal; and

7 the second portion of data is sampled by the memory
8 device synchronously with respect to the second external
9 clock signal.

10 ¹⁵~~165~~. The method of claim ¹⁴~~164~~ wherein the first and second
11 external clock signals are small voltage swing signals.

12 ⁹¹⁶~~166~~. A memory controller for controlling a synchronous memory
13 device, the memory controller comprising:

14 output driver circuitry to output data wherein:

15 the output driver circuitry outputs a first portion of
16 data in response to a rising edge transition of a first
17 external clock signal; and

18 the output driver circuitry outputs a second portion
19 of data in response to a falling edge transition of the
20 first external clock signal.

1 167. The memory controller of claim 166 further including:
2 multiplexer circuitry coupled to the output driver circuitry,
3 wherein:

4 in response to the first transition of the external clock
5 signal, the multiplexer circuitry couples the first portion of
6 data to an input of the output driver circuitry; and

7 in response to the second transition of the external
8 clock signal, the multiplexer circuitry couples the second
9 portion of data to the input of the output driver circuitry.

1 ~~168~~. The memory controller of claim ~~167~~ further including a
2 delay lock loop circuit coupled to the external clock signal, the
3 delay lock loop circuit generating a first internal clock signal,
4 wherein the multiplexer circuitry couples the first portion of data
5 to ~~the input of~~ the output driver circuitry in response to the
6 first internal clock signal.

1 ~~169~~. The memory controller of claim ~~168~~ wherein the delay lock
2 loop circuit generates a second internal clock signal, wherein the
3 multiplexer circuitry couples the second portion of data to the
4 ~~input of the~~ output driver circuitry in response to the second
5 internal clock signal.

1 ~~170~~. The memory controller of claim ~~166~~ wherein both the
2 rising edge transition of the first external clock signal and the

3 falling edge transition of the external clock signal transpire in
4 one clock cycle of the first external clock signal.

1 ²¹~~171~~. The memory controller of claim ¹⁶~~166~~ wherein both the
2 rising and falling edge transitions of the first external clock
3 signal include voltage swings of less than one volt.

1 ^{Sub C2} 172. A memory controller for controlling a synchronous memory
2 device, the memory controller comprising:

3 output driver circuitry to output data wherein:

4 the output driver circuitry outputs a first portion
5 of data in response to a first external clock signal; and

6 the output driver circuitry outputs a second portion
7 of data in response to a second external clock signal.

1 173. The memory controller of claim 172, further including:
2 multiplexer circuitry coupled to the output driver circuitry,
3 wherein:

4 in response to the first external clock signal, the
5 multiplexer circuitry couples the first portion of data
6 to an input of the output driver circuitry; and

7 in response to the second external clock signal, the
8 multiplexer circuitry couples the second portion of data
9 to the input of the output driver circuitry.